Doug **Reed**

Chip Designer · SoC Microarchitect

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Skills

Code SystemVerilog, Perl, Python, C, Clojure (kinda), Git.

/etc Linux, coffee roasting, bread baking, Rubik's cubes, distance running, swing dancing, guitar.

Experience

Intel Corporation — Austin, TX

Principal Engineer, Advanced Architecture Development Group — *2021 - present*

- REDACTED.

Centaur Technology — Austin, TX

Design Engineer/Microarchitect — *2014 - 2021*

- Architected & implemented a new mid-level cache and a ring interconnect for a high performance x86 microprocessor.
- Integrated new cache and interconnect modules into existing legacy design.
- Implemented best-known academic prefetchers in RTL.
- Created a framework for transactional debugging of MP memory fails.
- Helped define verification plan for cache hierarchy.
- Led an effort to modernize various design and verification methodologies.
- Wrote tools to enable faster/easier ECOs for incremental tapeouts, and performed the gates edits.

Centaur Technology — Austin, TX

Logic Design Engineer — *2012 - 2014*

- Primary maintainer of the LLC in a high performance x86 processor.
- Architected and implemented new features for performance, debuggability, and error detection and recovery.

Centaur Technology — Austin, TX

Architectural Validation Engineer — *2009 - 2012*

- Contributed to and developed hardware emulation and diagnostic utilities in C, C++, and x86 assembly.
- Architected and implemented functional coverage methodology and block-level functional equivalence checking for FPGA-targeted RTL.
- Designed Centaur's first SystemVerilog-based test bench for our LLC.

Education

The University of Texas — Austin, TX

MSEE – Computer Architecture and Embedded Processors — *2010-2015*

- MS Report: Performance and Complexity Tradeoffs in Partially-Inclusive Caches
- Supervised by Professor Vijay Reddi

The University of Texas — Austin, TX

BSEE – Computer Engineering — *2005-2009*

- Design Project: FPGA-Accelerated Hardware Verification.

Selected Patents (30 total)

Deadlock/livelock resolution using service processor	9,575,816
Cache replacement policy that considers memory access type	9,652,398
Conditional pattern detector for detecting hangs	9,753,799
Cache management request fusing	9,892,803
Pattern detector for detecting hangs	9,946,651
Sanitize-aware DRAM controller	9,972,375
Processor with programmable prefetcher [...]	10,268,586
Distributed hang recovery logic	10,324,842
Dynamic cache replacement way selection based on address tag bits	10,698,827
[Cache configurable to] allocate into all or a subset of its ways [...]	10,719,434

More patents available here: https://bit.ly/1nv3nt0r